DATA SHEET

SAA4960
Integrated PAL comb filter

Preliminary specification
File under Integrated Circuits, IC02

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Philips
Semiconductors

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Integrated PAL comb filter SAA4960

FEATURES

- One chip adaptive PAL comb filter
- Time discrete but continuous amplitude signal processing with analog interfaces
- Internal delay lines, filters, clock processing and signal switches
- Alignment-free
- No hanging dots or residual cross colour on vertical transients
- Few external components.

GENERAL DESCRIPTION

The SAA4960 is an adaptive alignment-free one chip comb filter compatible with PAL systems and provides high performance in Y/C separation.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.75	5	5.5	V
V_{DDD}	digital supply voltage	4.75	5	5.5	V
V_{CCO}	analog supply voltage output buffer	4.75	5	5.5	V
V_{CCPLL}	analog supply voltage PLL	4.75	5	5.5	V
I_{CCO}	analog supply current output buffer	–	70	90	mA
I_{DDD}	digital supply current	–	10	20	mA
I_{CCA}	analog supply current	–	35	40	mA
I_{CCPLL}	analog supply current PLL	–	1.5	3.0	mA
$V_{17(p-p)}$	CVBS and Y input signal (peak-to-peak value)	0.7	1	1.4	V
$V_{10(p-p)}$	chrominance input signal (peak-to-peak value)	–	0.7	1	V
$V_{1(p-p)}$	subcarrier input signal (peak-to-peak value)	100	200	400	mV
$V_{14(p-p)}$	luminance output signal (peak-to-peak value)	0.6	1	1.54	V
$V_{12(p-p)}$	chrominance output signal (peak-to-peak value)	–	0.7	1.1	V
$V_{15(p-p)}$	CVBS and Y output signal (peak-to-peak value)	0.6	1	1.54	V

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA4960	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1

BLOCK DIAGRAM

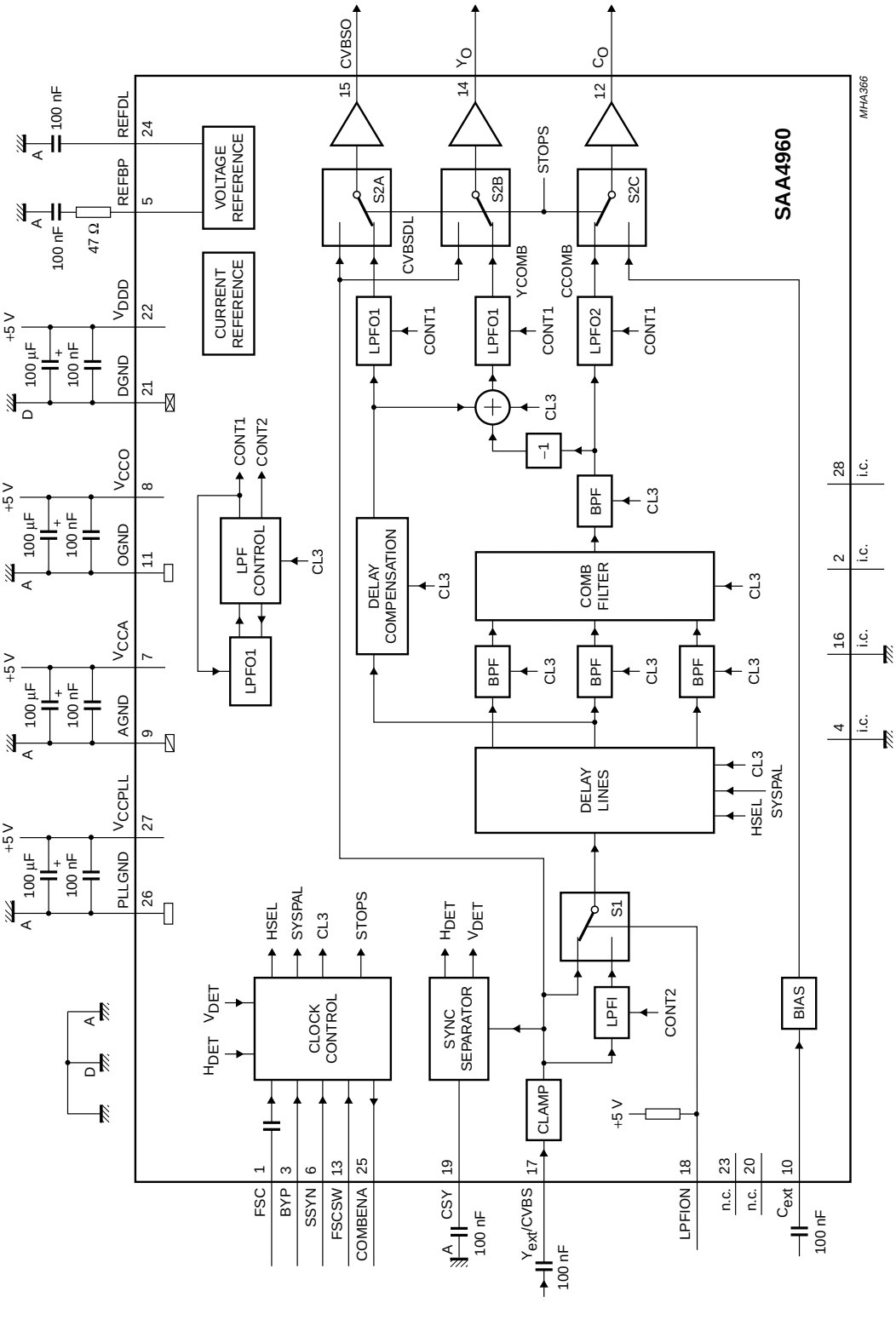


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FSC	1	subcarrier frequency input
i.c.	2	internally connected
BYP	3	bypass mode forcing input
i.c.	4	internally connected
REFBP	5	decoupling capacitor for band-pass filter reference
SSYN	6	bypass definition input
V_{CCA}	7	analog supply voltage
V_{CCO}	8	analog supply voltage output buffer
AGND	9	analog ground (signal reference)
C_{ext}	10	external chrominance input signal
OGND	11	analog ground output buffer
C_O	12	chrominance output signal
FSCSW	13	f_{sc} reference selection input
Y_O	14	luminance output signal
CVBSO	15	uncombed CVBS output signal
i.c.	16	internally connected
Y_{ext}/CVBS	17	CVBS (VBS) input signal
LPFION	18	disable alias-filter
CSY	19	storage capacitor
n.c.	20	not connected
DGND	21	digital ground
V_{DDD}	22	digital supply voltage
n.c.	23	not connected
REFDL	24	decoupling capacitor for delay lines
COMBENA	25	COMB-mode output signal
PLLGND	26	analog ground PLL
V_{CCPLL}	27	analog supply voltage PLL
i.c.	28	internally connected

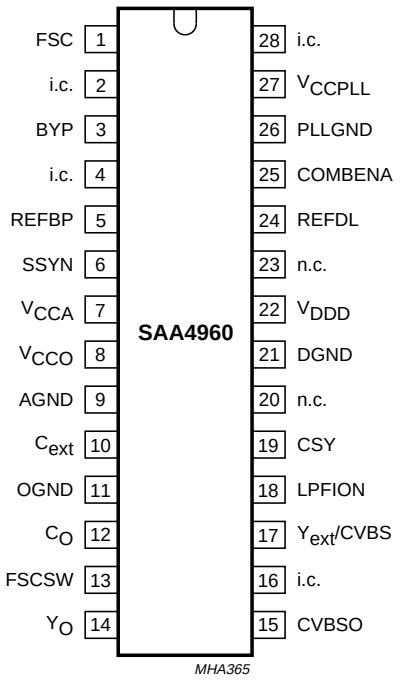


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Functional requirements

The PAL comb filter processes the video standards PAL B, G and H. PAL D and I signals can also be processed but with the drawback of a slightly reduced bandwidth.

For SECAM and SVHS signals, the input signals can be bypassed to the output without processing by selecting the BYPASS-mode.

A sync separation circuit is incorporated to generate control signals for the internal clock processing. With a sync compression of up to 12 dB the sync separator works properly (see Fig.4).

The IC is controlled via four pins:

1. BYP forces the IC into the BYPASS-mode (comb filter function off)
2. SSYN defines whether the COMB-mode is entered synchronously or not and defines the polarity of the BYP pin
3. FSCSW selects the reference frequency f_{sc} or $2 \times f_{sc}$
4. LPFION enables the internal pre-filter.

It is possible to select the following modes of operation:

COMB-mode: Luminance and chrominance comb filter function active if BYPASS-mode not active.

BYPASS-mode: Signal processing not active, all clocks inactive, C_{ext} (pin 10) is bypassed to C_O (pin 12) and Y_{ext}/CVBS (pin 17) is bypassed to Y_O (pin 14) and CVBSO (pin 15). This mode is forced via BYP (pin 3).

If the stimulus of the mode is changed, the IC is following the new mode after the stabilization time given in Table 1.

Table 1 Stabilization time after mode change

MODE CHANGE	MAXIMUM STABILIZATION TIME
COMB-mode to BYPASS-mode	1 line
BYPASS-mode to COMB-mode	1 field

The mode change from BYPASS to COMB depends on SSYN (pin 6) and can be asynchronous or synchronous related to the vertical pulse. The mode change from COMB to BYPASS is always performed asynchronously.

Pin description

FSC (PIN 1)

Input for the reference frequency f_{sc} (see note 2 of Chapter “Characteristics”) or $2 \times f_{sc}$. For SECAM standard signals the best signal performance in BYPASS-mode is achieved by switching the FSC input signal off externally.

BYP (PIN 3)

Input signal that controls the operation mode. A low-pass filter is added to the input for suppression of subcarrier frequencies. Thus applications are supported where the operation mode (COMB or BYPASS) is controlled by the DC-level of the FSC input signal at pin 1. For those applications the BYP input can be externally connected to FSC (pin 1).

Depending on SSYN (pin 6) the function of BYP can be adapted to a certain application with respect to the polarity of the logic level and with respect to the behaviour when entering the COMB-mode.

Dependent on SSYN the BYP input can be either inverted or non-inverted with the function as shown in Table 2:

Table 2 Bypass function

SSYN	BYP	SELECTED MODE
LOW	LOW	COMB-mode
LOW	HIGH	BYPASS-mode
HIGH	LOW	BYPASS-mode
HIGH	HIGH	COMB-mode

Dependent on SSYN the behaviour when entering the COMB-mode is different for the both selectable logic polarities while the BYPASS-mode is always entered asynchronously (immediately).

Table 3 Behaviour when entering the COMB-mode

SSYN	ENTERING COMB-MODE
LOW	immediately if BYP = LOW
HIGH	synchronized by vertical pulse if BYP = HIGH

The PLL and the clock processing are always stopped if the selected level for BYPASS is applied to BYP (independent of the vertical pulse).

REFBP (PIN 5)

Decoupling capacitor for the band-pass filter reference voltage.

SSYN (PIN 6)

Input signal that controls the function of BYP (pin 3).

V_{CCA}, V_{CCO}, V_{DDD} AND V_{CCPLL} (PINS 7, 8, 22 AND 27)

Supply voltages.

AGND, OGND, DGND AND PLLGND (PINS 9, 11, 21 AND 26)

Ground connection. AGND is used as signal reference for all analog input and output signals.

C_{ext} (PIN 10)

Input for an external chrominance signal which is correlated to the external VBS signal.

C_O (PIN 12)

Chrominance output signal. This output can be switched between the comb filtered chrominance from the CVBS signal and the external chrominance signal from the input C_{ext} if the IC is forced into BYPASS-mode.

Table 4 C_O output signal

MODE	C_O OUTPUT SIGNAL
COMB	comb filtered chrominance signal
BYPASS	external chrominance signal of C_{ext} input

FSCSW (PIN 13)

Input signal to select between f_{sc} or $2 \times f_{sc}$ as reference at the FSC input pin.

Table 5 Reference frequency selection

FSCSW	SELECTED REFERENCE
HIGH	$2 \times f_{sc}$
LOW	f_{sc}

Y_O (PIN 14)

VBS output signal. This output can be switched between the comb filtered luminance signal (including synchronization) and the external (C)VBS signal from the input Y_{ext}/CVBS. In COMB-mode the output signal is delayed by 2 lines and by an additional processing delay.

Table 6 Y_O output signal

MODE	Y_O OUTPUT SIGNAL
COMB	comb filtered luminance signal
BYPASS	external CVBS signal of Y_{ext}/CVBS input

CVBSO (PIN 15)

CVBS output signal directly from the input in BYPASS-mode or delayed by the signal processing time of 2 lines and an additional processing delay.

Table 7 CVBSO output signal

MODE	CVBSO OUTPUT SIGNAL
COMB	delay compensated CVBS signal
BYPASS	external CVBS signal of Y_{ext}/CVBS input

Y_{ext}/CVBS (PIN 17)

Input for the CVBS signal or for an external VBS signal.

LPFION (PIN 18)

Input signal to disable the internal pre-filter LPFI.

Table 8 Pre-filter mode

LPFION	SELECTED MODE
LOW	LPFI inactive
HIGH	LPFI active
Floating	LPFI active

CSY (PIN 19)

Sync top capacitor for the sync separator.

REFDL (PIN 24)

Decoupling capacitor for the delay line reference voltage.

COMBENA (PIN 25)

Output signal that indicates the current mode of operation. This output is forced to LOW if the comb filter is in BYPASS-mode.

Table 9 Mode of operation

COMBENA	SELECTED MODE
LOW	BYPASS-mode; PLL and clock processing stopped
HIGH	COMB-mode

Internal functional description

SWITCHED CAPACITOR DELAY LINE

Delays the CVBS input signal by 2 lines and 4 lines. Input signals for the delay lines are the CVBS signal, the clock CL3 ($3 \times f_{sc}$), the control signal HSEL and the standard selection signal SYSPAL.

Output signals are the non-delayed, the 2-line delayed and the 4-line delayed CVBS signal.

SWITCHED CAPACITOR BAND-PASS FILTERS (BPF)

The comb filter input BPFs attenuate the low frequencies to guarantee a correct signal processing within the logical comb filter.

The comb filter output BPF reduces the alias components that are the result of the non-linear signal processing within the logical comb filter.

LOGICAL COMB FILTER

Separates the chrominance from the band-pass filtered CVBS signal.

COMPENSATION DELAY

Compensates the internal processing time of the band-pass filters and the logical comb filter section.

ADDER

The comb filtered luminance output signal is obtained by adding the delayed CVBS signal and the inverted comb filtered chrominance signal.

LOW-PASS FILTER INPUT (LPFI)

Analog input low-pass filter to reduce the outband frequencies of EMC. The input low-pass filter is included in the signal path but it can be switched off via the input signal LPFION.

LOW-PASS FILTER OUTPUT (LPFO1 AND LPFO2)

Two different types of output low-pass filters (LPFO1 and LPFO2) are necessary to get equal signal delays within the luminance path and the chrominance path (important for good transient behaviour). The low-pass output filter type LPFO1 is used for the luminance output while LPFO2 is used for the chrominance output. The filters are analog 3rd order elliptic low-pass filters that convert the output signals from the time discrete to the time continuous domain (reconstruction filter).

LPF CONTROL

Automatic tuning of the low-pass filters is achieved by adjusting the filter delays. The control information for all filters (CONT1 and CONT2) is derived from a built-in reference filter (LPFO1-type) that is part of a control loop. The control loop tunes the reference filter delay and thus all other filter delays to a time constant derived from the system clock CL3.

CONTROL AND CLOCK PROCESSING (CLOCK CONTROL)

The control and clock processing block (see Fig.7) consists of the sub-blocks PLL, the clock processing and the mode control. The PLL and the clock processing are released for operation if the input level at BYP selects the COMB-mode.

Main tasks of the control and clock processing are:

- Clock generation of system clock CL3
- Delay line start control
- Mode control.

The signal processing is based on a $3 \times f_{sc}$ system clock (CL3), that is generated by the clock processing from the f_{sc} signal at FSC (pin 1) via a PLL. Because the subcarrier frequency divided by the line frequency results not in an integer value a clock phase correction of 180° is necessary every second line for PAL standards. The clock phase correction is controlled by the input signals horizontal sync. Additionally the delay line start is synchronized once a field to the input signals horizontal sync. The 25 Hz PAL offset is corrected in this way.

The PLL provides a master clock MCK of $6 \times f_{sc}$, which is locked to the subcarrier frequency at FSC (pin 1).

The system clock CL3 ($3 \times f_{sc}$) is obtained from MCK by a divide-by-two circuit. The 180° phase shift is generated by stopping the divide-by-two circuit for one MCK clock cycle.

The generated clock is a pseudo-line-locked clock that is referenced to f_{sc}. The sync separator generates the necessary signals H_{DET} and V_{DET} indicating the line (H) and the field (V) sync periods.

The current mode of operation (BYPASS or COMB) is external readable via COMBENA (pin 25).

The input signals of the control and clock processing (CLOCK CONTROL) are:

H_{DET}: analog horizontal pulse from sync separator

V_{DET}: analog vertical pulse from sync separator

FSC: subcarrier frequency (f_{sc} or $2 \times f_{sc}$)

FSCSW: reference frequency selection

BYP: BYPASS control signal

SSYN: vertical synchronous mode selection for BYP and polarity selection of BYP.

The output signals are:

CL3: system clock ($3 \times f_{sc}$)

HSEL's: line start signals for the delay lines

STOPS: forces the comb filter via the switches S2A, S2B and S2C into the BYPASS-mode (always asynchronous) or COMB-mode (synchronous or asynchronous with V_{INT}; depending on SSYN)

COMBENA: HIGH during COMB-mode; otherwise LOW.

Table 10 Function of STOPS signal

STOPS-STATE	SELECTED MODE
LOW	COMB
HIGH	BYPASS

HORIZONTAL AND VERTICAL SYNC SEPARATOR

A build-in sync separator circuit generates the H_{DET} and V_{DET} signals from the Y_{ext}/CVBS input signal. This circuit is still working properly at input signals with a 12 dB attenuated sync in a normal 700 mV black-to-white video signal (see Fig.4).

CLAMP

The black level clamping of the video input signal is performed by the sync separator stage. The clamping level is nearly adequate to the voltage at REFDL (pin 24).

SIGNAL SWITCH S1

The switch is included to bypass the low-pass input filter.

For the CVBS input of the delay line block two signals can be selected via the slow signal switch S1.

Table 11 Function of signal switch S1

LPFION-STATE	DELAY LINE INPUT
LOW	non-pre-filtered input signal Y_{ext}/CVBS
HIGH	pre-filtered input signal Y_{ext}/CVBS
Floating	pre-filtered input signal Y_{ext}/CVBS

SIGNAL SWITCH S2A

For the CVBSO output two signals can be selected via the signal switch S2A.

Table 12 CVBSO output signal

STOPS-STATE	CVBSO OUTPUT SIGNAL	MODE
LOW	delayed input CVBSDL	COMB
HIGH	non-delayed input Y_{ext}/CVBS	BYPASS

SIGNAL SWITCHES S2B AND S2C

Two switches are included to bypass the comb filter signal processing. The input video signal C_{ext} for the switch S2C is internally biased.

For the Y_O output two signals can be selected via S2B.

Table 13 Y_O output signal

STOPS-STATE	Y_O OUTPUT SIGNAL	MODE
LOW	YCOMB (combed luminance)	COMB
HIGH	input Y_{ext}/CVBS	BYPASS

For the C_O output two signals can be selected via S2C.

Table 14 C_O output signal

STOPS-STATE	C_O OUTPUT SIGNAL	MODE
LOW	CCOMB (combed chrominance)	COMB
HIGH	input C_{ext}	BYPASS

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–	6.5	V
V	input voltage protection threshold	except pin 1	–0.3	V_{CC} + 0.3	V
I_{CC}	total supply current		–	155	mA
I_O	output current (C_O, Y_O and CVBSO)		–	±15	mA
	output current (COMBENA)		–	10	mA
P_{tot}	total power dissipation		–	900	mW
T_{amb}	operating ambient temperature		0	70	°C
T_{stg}	storage temperature		–25	+150	°C
V_{es}	electrostatic handling	note 1			

Note

1. Human Body Model: C = 100 pF; R = 1.5 kΩ; V = 2 kV; charge device model: C = 200 pF; R = 0 Ω; V = 300 V.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	31	K/W

CHARACTERISTICS

$V_{DDD} = V_{CCA} = V_{CCO} = V_{CCPLL} = 5$ V; $T_{amb} = 25$ °C; input signal Y_{ext}/CVBS = 1 V (p-p) (0 dB); input signal C = 0.7 V (p-p) (0 dB); input signal FSC = 200 mV (p-p), sine wave, DC level = 2 V; input signal LPFION = 5 V; test signal: EBU colour bar 100/0/75/0 *"CCIR471-1"*; source impedance for Y_{ext}/CVBS, C_{ext} = 75 Ω decoupled with 100 nF; source impedance for FSC = 75 Ω; load impedance for CVBSO, Y_O, C_O = 1 kΩ and 20 pF in parallel; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltage						
V_{CCA}	analog supply voltage (pin 7)	note 1	4.75	5	5.5	V
V_{CCO}	analog supply voltage output buffer (pin 8)	note 1	4.75	5	5.5	V
V_{DDD}	digital supply voltage (pin 22)	note 1	4.75	5	5.5	V
V_{CCPLL}	analog supply voltage PLL (pin 27)	note 1	4.75	5	5.5	V
FSC (pin 1)						
$V_{1(p-p)}$	input AC voltage (peak-to-peak value)		100	200	400	mV
	input AC voltage is valid for sine wave square wave		 – 0.4	 – 0.5	 – 0.6	 – duty cycle
V_1	input DC level		0	–	5.3	V
C_1	input capacitance		–	–	10	pF
I_{leak}	input leakage current		–	–	10	μA
Z_1	source impedance		–	–	800	Ω
BYP (pin 3)						
V_{IH}	HIGH level input voltage		2.4	–	V_{CC}	V
V_{IL}	LOW level input voltage		0	0.85	1.5	V
I_{leak}	input leakage current		–	–	10	μA
C_3	input capacitance		–	–	10	pF
REFBP (pin 5)						
V_5	DC voltage		1.1	1.25	1.4	V
SSYN (pin 6)						
V_{IH}	HIGH level input voltage		2.4	–	V_{CC}	V
V_{IL}	LOW level input voltage		0	0.85	1.5	V
I_{leak}	input leakage current		–	–	10	μA
C_6	input capacitance		–	–	10	pF
V_{CCA} (pin 7)						
I_{CCA}	analog supply current		–	35	40	mA
V_{CCO} (pin 8)						
I_{CCO}	supply current		–	70	90	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{ext} (pin 10)						
V_{10}	input voltage (AC coupled)		–	0	3	dB
R_{10}	input resistance	1.25 V	500	700	1000	kΩ
C_{10}	input capacitance		–	–	10	pF
Z_{10}	source impedance		–	–	1	kΩ
C_O (pin 12)						
V_{10}/V_{12}	BYPASS-mode: C_O/C_{ext}	$f_{sc} \pm 0.3f_{sc}$; note 2	–1	0	+1	dB
COMB-mode: transfer function C-path see Fig.8						
V_{12}	DC offset voltage related to input		–400	0	+400	mV
$\lvert\Delta V_{12}\rvert$	DC jump when forcing into BYPASS-mode		–	100	450	mV
R_{12}	output resistance		–	10	100	Ω
R_L	load resistance (to ground)		0.3	–	–	kΩ
C_L	load capacitance (to ground)		–	–	25	pF
V_{17}/V_{12}	suppression (comb depth)	see Fig.5 and note 3				
		$283 \times f_H$	26	30	–	dB
		$(283 - 43) \times f_H$	20	24	–	dB
		$(283 + 35) \times f_H$	20	24	–	dB
FPN	fixed pattern noise for divided clock frequencies referenced to 0.7 V (p-p)	$0.75f_{sc}$	–	–	–30	dB
		f_{sc}	–	–	–50	dB
		$1.5f_{sc}$	–	–	–37	dB
		$2f_{sc}$	–	–	–30	dB
α_{cr}	crosstalk suppression at vertical transients no-colour ↔ colour	see Fig.3	26	30	–	dB
S/N	signal-to-noise ratio (0.7 V/V_{eff} noise)	unweighted; $f_{sc} \pm 0.3f_{sc}$; note 2	56	72	–	dB
α_{cr}	crosstalk between different inputs	0 to 5 MHz	–	–60	–40	dB
$V_{12(p-p)}$	FSC residue in BYPASS-mode related to 700 mV (p-p)		–	–	–60	dB
G_d	differential gain		0.95	–	–	
FSCSW (pin 13)						
V_{IH}	HIGH level input voltage		2	–	V_{CC}	V
V_{IL}	LOW level input voltage		0	–	0.8	V
C_{13}	input capacitance		–	–	10	pF
I_{leak}	input leakage current		–	–	10	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Y_O (pin 14)						
V_{14}/V_{17}	BYPASS-mode: C_O/C_{ext}	0 to 5 MHz	–1	0	+1	dB
COMB-mode: transfer function Y-path see Fig.9						
V_{14}	DC offset voltage related to input		–400	0	+400	mV
$\lvert\Delta V_{14}\rvert$	DC jump when forcing into BYPASS-mode		–	200	450	mV
R_{14}	output resistance		–	10	100	Ω
R_L	load resistance (to ground)		0.3	–	–	kΩ
C_L	load capacitance (to ground)		–	–	25	pF
V_{17}/V_{14}	suppression (comb depth)	see Fig.6 and note 3				
		$283.75 \times f_H$	26	30	–	dB
		$(283.75 - 43) \times f_H$	10	12	–	dB
		$(283.75 + 35) \times f_H$	18	24	–	dB
FPN	fixed pattern noise for divided clock frequencies referenced to 0.7 V (p-p) black-to-white	$0.75f_{sc}$	–	–	–40	dB
		f_{sc}	–	–	–30	dB
		$1.5f_{sc}$	–	–	–30	dB
		$2f_{sc}$	–	–	–20	dB
α_{cr}	crosstalk suppression at vertical transients gray ↔ multi-burst	see Fig.3	26	30	–	dB
S/N	signal-to-noise ratio (0.7 V/V_{eff} noise)	unweighted; 200 kHz to 5 MHz	56	72	–	dB
α_{cr}	crosstalk between different inputs	0 to 5 MHz	–	–60	–40	dB
$V_{14(p-p)}$	FSC residue in BYPASS-mode related to 700 mV (p-p)		–	–	–60	dB
G_d	differential gain		0.95	–	–	
CVBSO (pin 15)						
V_{15}/V_{17}	BYPASS-mode: CVBSO/CVBS	0 to 5 MHz	–1	0	+1	dB
COMB-mode: transfer function CVBS-path see Fig.9						
V_{15}	DC offset voltage		–400	0	+400	mV
$\lvert\Delta V_{15}\rvert$	DC jump when forcing into BYPASS-mode		–	200	450	mV
R_{15}	output resistance		–	10	100	Ω
R_L	load resistance (to ground)		0.3	–	–	kΩ
C_L	load capacitance (to ground)		–	–	25	pF
FPN	fixed pattern noise for divided clock frequencies referenced to 0.7 V (p-p) black-to-white	$0.75f_{sc}$	–	–	–40	dB
		f_{sc}	–	–	–30	dB
		$1.5f_{sc}$	–	–	–30	dB
		$2f_{sc}$	–	–	–20	dB
S/N	signal-to-noise ratio (0.7 V/V_{eff} noise)	unweighted; 200 kHz to 5 MHz	56	72	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α_{cr}	crosstalk between different inputs	0 to 5 MHz	–	–60	–40	dB
$V_{15(p-p)}$	FSC residue in BYPASS-mode related to 700 mV (p-p)		–	–	–60	dB
G_d	differential gain		0.95	–	–	
P_d	differential phase		–	2	3	deg
Y_{ext}/CVBS (pin 17)						
V_{17}	input voltage (AC coupled)	12 dB sync attenuation possible; see Fig.4	–3	0	+3	dB
I_{17}	input current during sync pulse		–10	–8.0	–	µA
	input current during active video		–	0.84	1.5	µA
V_{17}	DC voltage during black level		1.1	1.25	1.4	V
Z_{17}	source impedance		–	–	1	kΩ
LPFION (pin 18)						
V_{IH}	HIGH level input voltage		2	–	V_{CC}	V
V_{IL}	LOW level input voltage		0	–	0.8	V
I_{18}	input current	0.8 V	–	8	20	µA
		2.0 V	–	8	20	µA
C_{18}	input capacitance		–	–	10	pF
CSY (pin 19)						
V_{19}	DC voltage		0	2.45	V_{CC}	V
V_{DDD} (pin 22)						
I_{DDD}	supply current		–	10	20	mA
REFDL (pin 24)						
V_{24}	DC voltage		1.1	1.25	1.4	V
COMBENA (pin 25)						
V_{OL}	LOW level output voltage	3 mA	0.26	0.4	0.55	V
V_{OH}	HIGH level output voltage		4	–	V_{CC}	V
I_{OH}	HIGH level output current	2.4 V	–55	–24	–	µA
V_{CCPLL} (pin 27)						
I_{27}	supply current		–	1.5	3	mA

Notes to the characteristics

1. $\Delta V = |V_{CCA} - V_{DDD}| \leq 300$ mV
   $\Delta V = |V_{CCA} - V_{CCO}| \leq 300$ mV
   $\Delta V = |V_{CCO} - V_{DDD}| \leq 300$ mV
   $\Delta V = |V_{CCA} - V_{CCPLL}| \leq 300$ mV
   $\Delta V = |V_{CCO} - V_{CCPLL}| \leq 300$ mV
   $\Delta V = |V_{DDD} - V_{CCPLL}| \leq 300$ mV
   All voltages are related to AGND.
2. Subcarrier frequency f_{sc} = 4.43361875 MHz.
3. Line frequency f_H = 15.625 kHz.

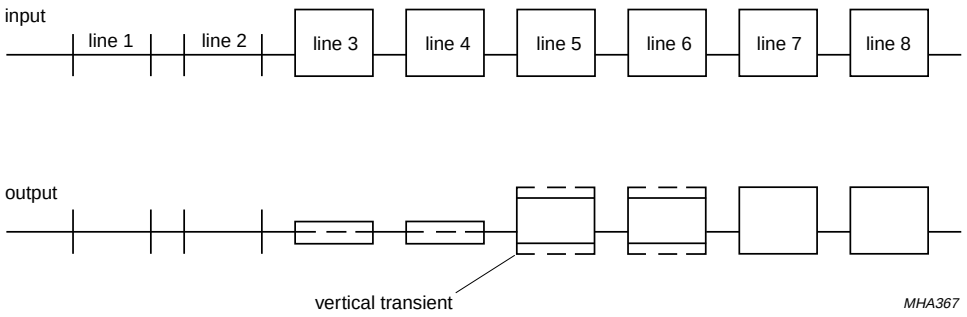


Fig.3 Vertical transmission by different video signals from line to line.

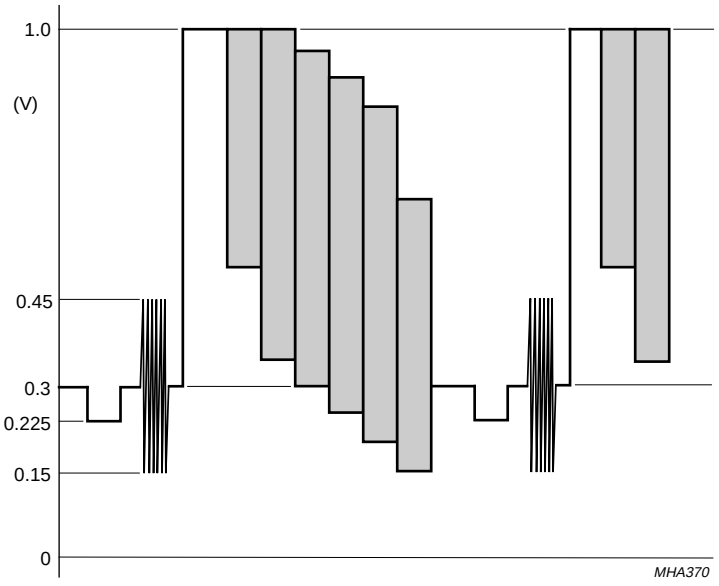


Fig.4 EBU colour bar 100/0/75/0 with 12 dB sync attenuation.

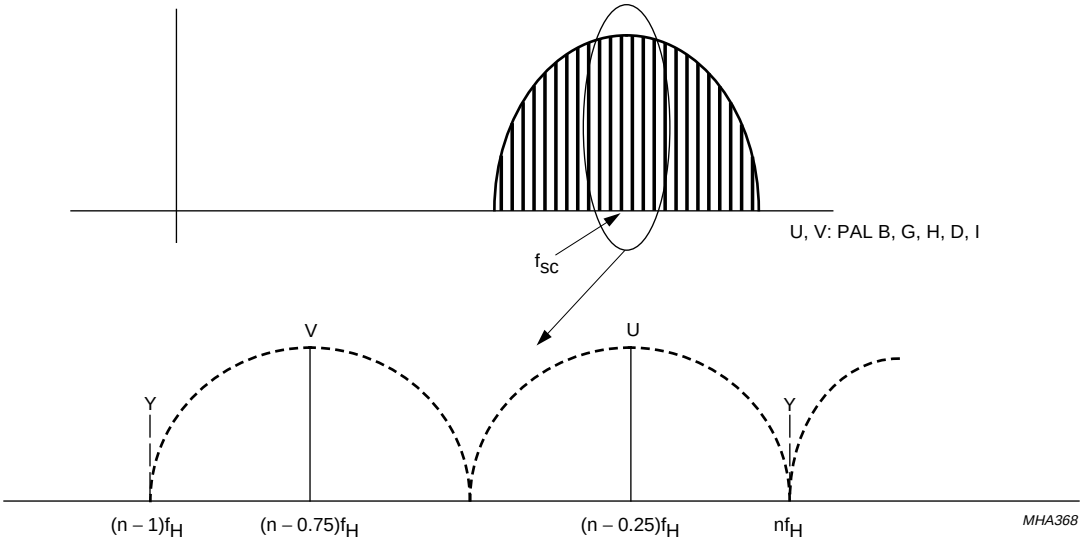


Fig.5 Principle frequency response of a comb filtered PAL chrominance signal.

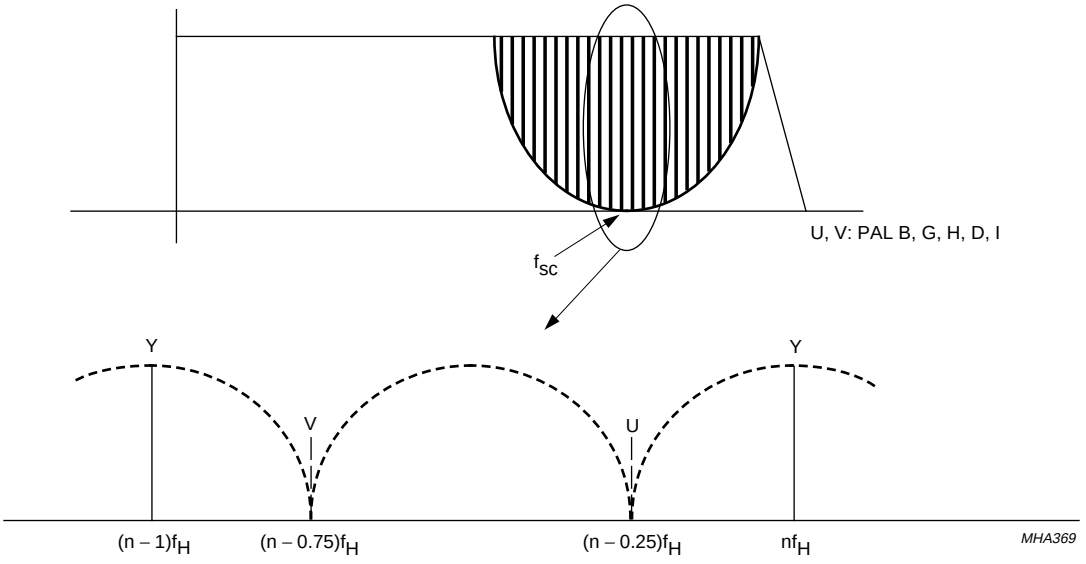


Fig.6 Principle frequency response of a comb filtered PAL luminance signal.

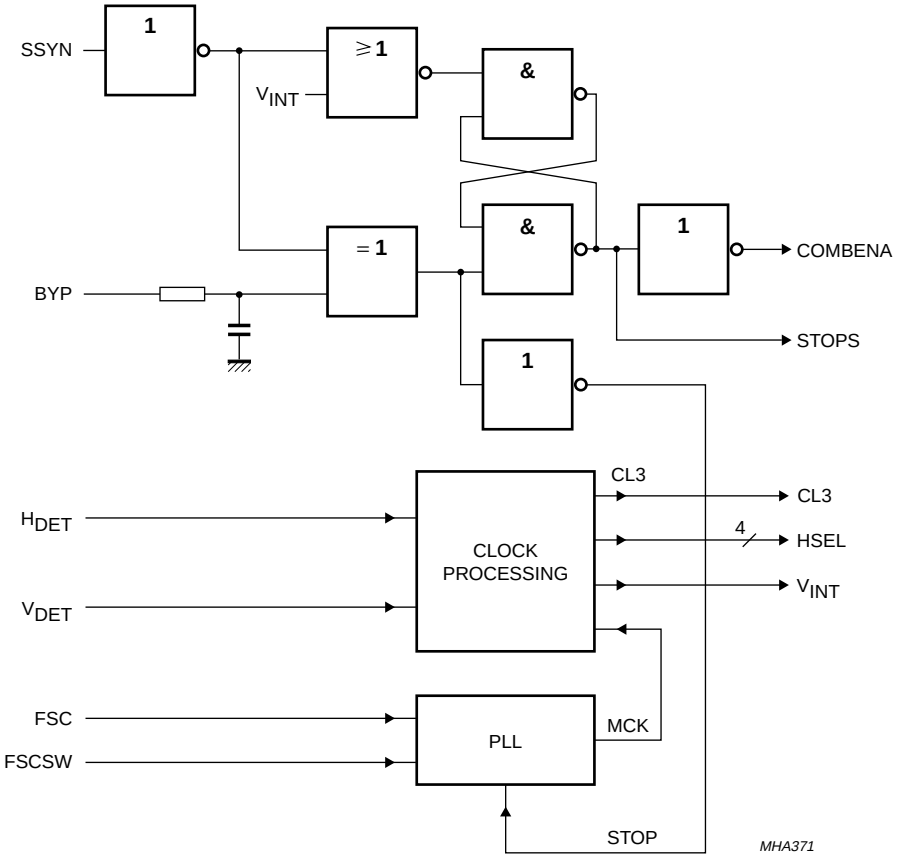


Fig.7 Clock control.

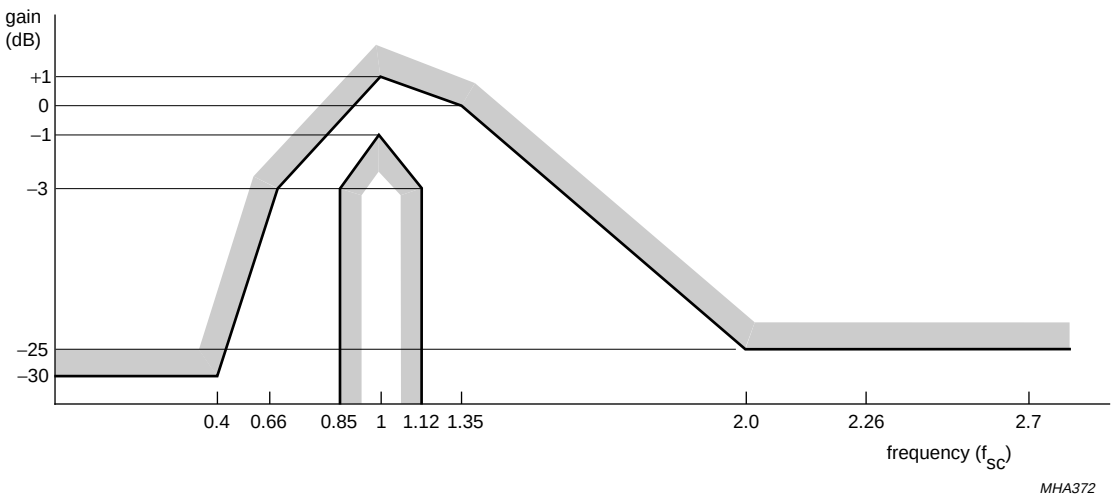


Fig.8 Chrominance path: tolerance band with anti-alias filter.

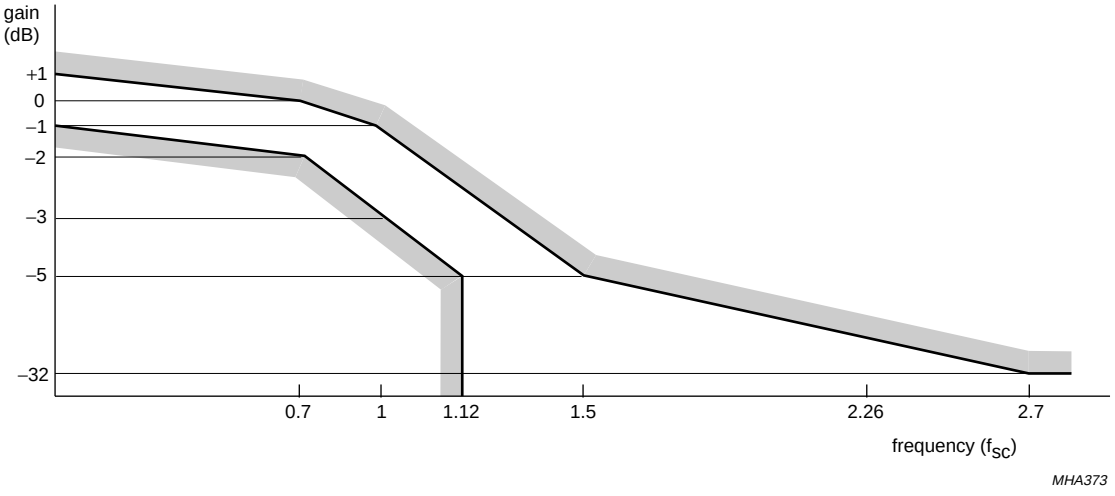


Fig.9 Luminance and CVBSO path: tolerance band with anti-alias filter.

TEST AND APPLICATION INFORMATION

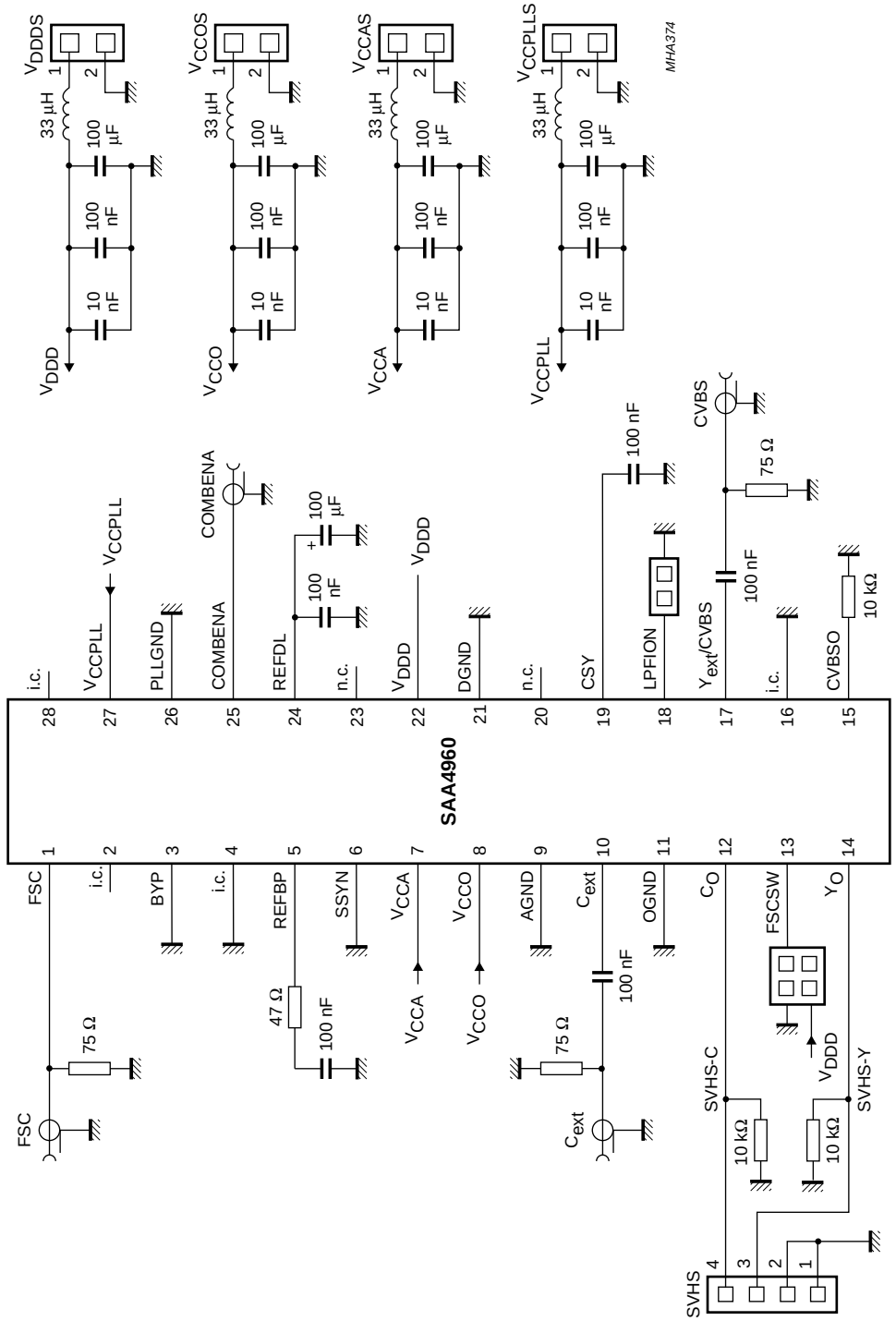


Fig.10 Test circuit.

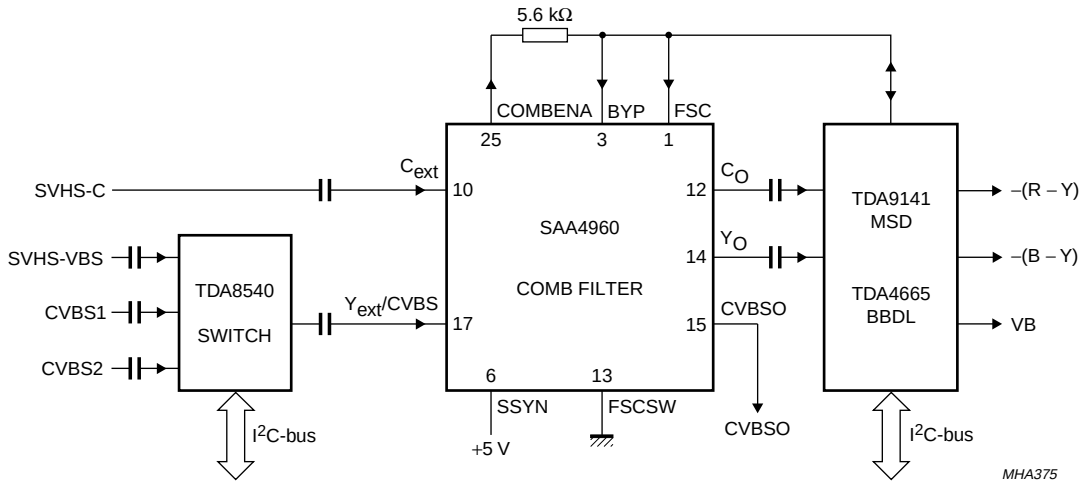


Fig.11 Application diagram: SAA4960 with TDA9141.

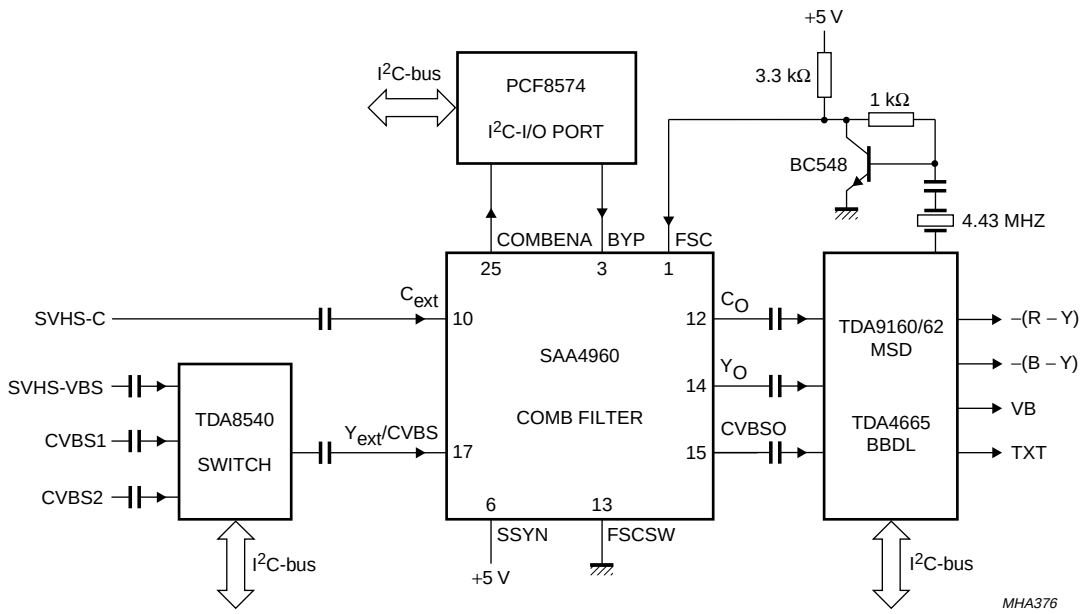


Fig.12 Application diagram: SAA4960 with TDA9160/62.

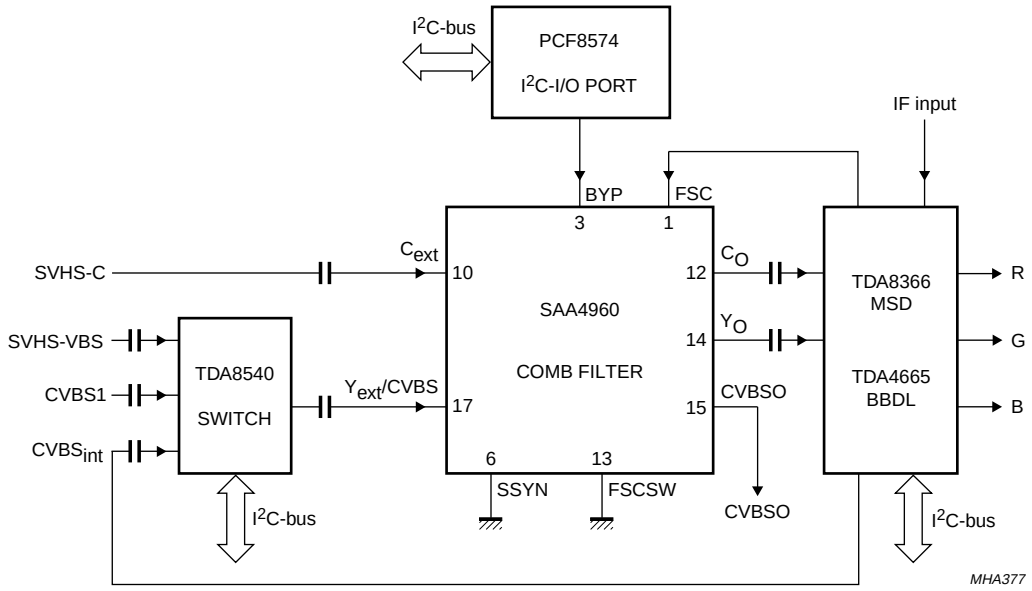
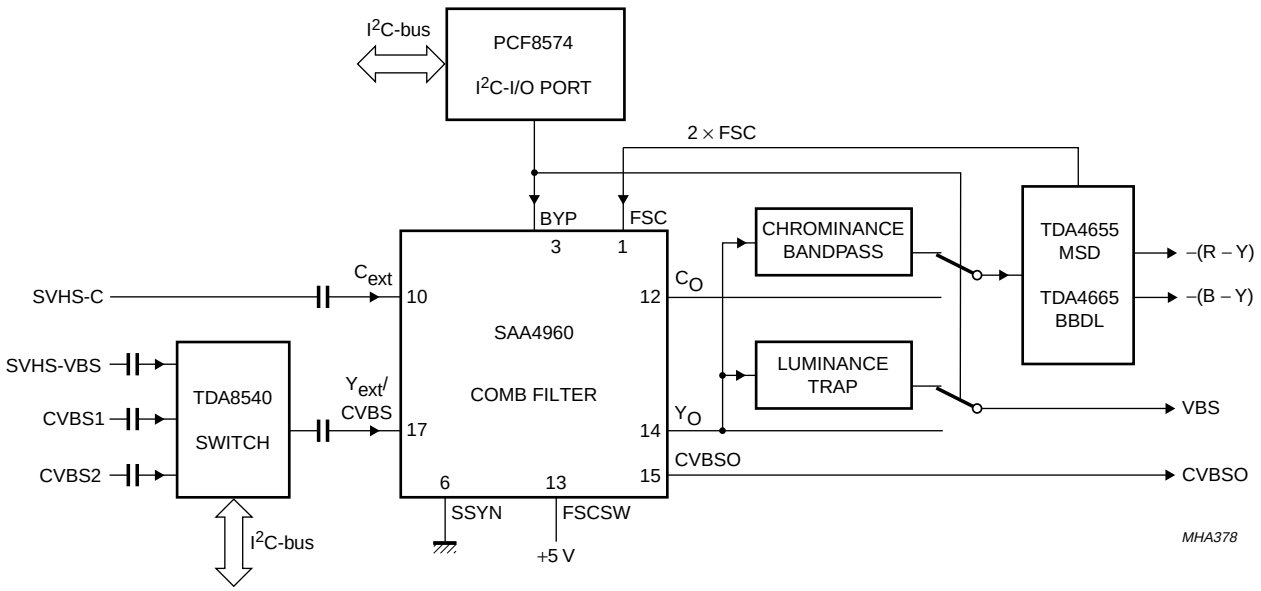


Fig.13 Application diagram: SAA4960 with TDA8366.

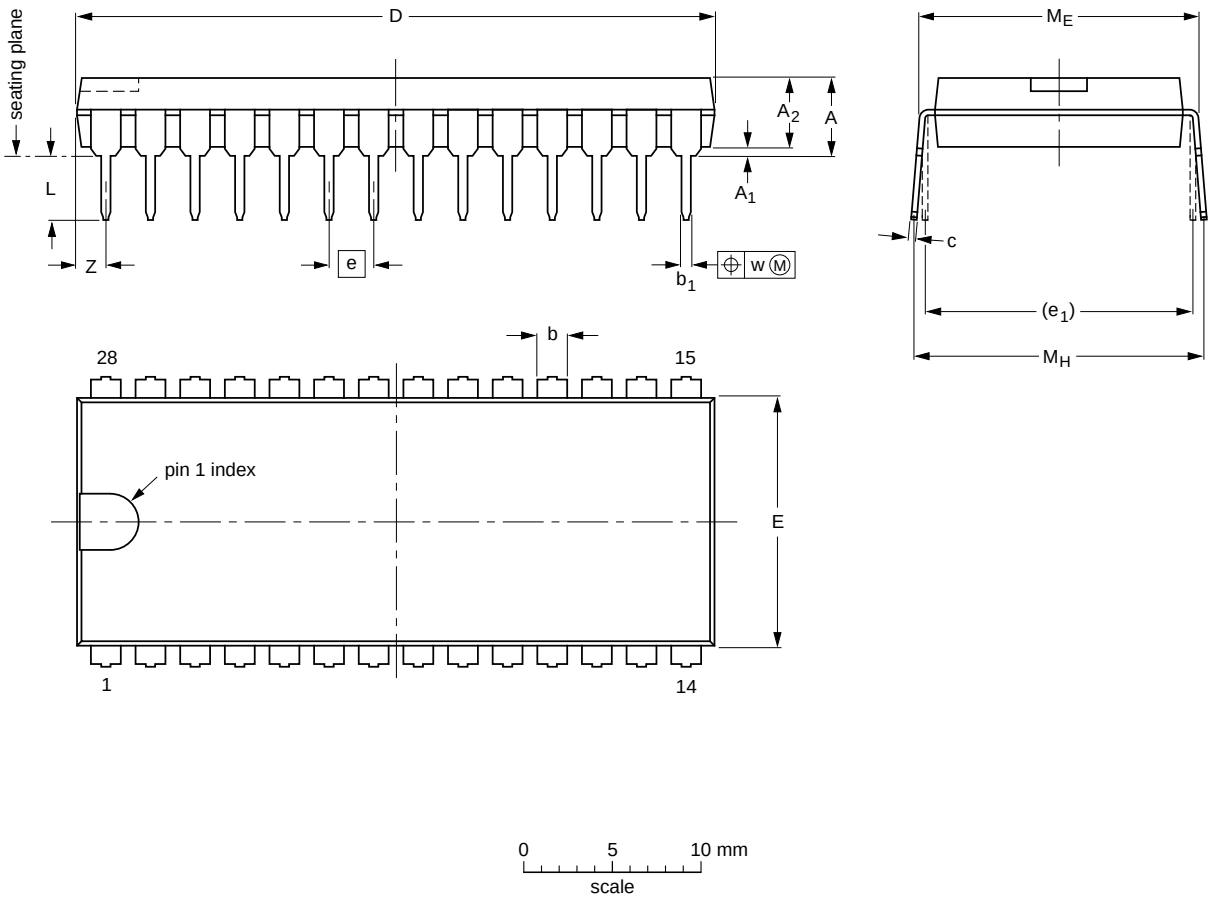


Remark: all switches in LOW position.

Fig.14 Application diagram: SAA4960 with TDA4655.

PACKAGE OUTLINE

DIP28: plastic dual in-line package; 28 leads (600 mil) **SOT117-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				~~92-11-17~~ 95-01-14

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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